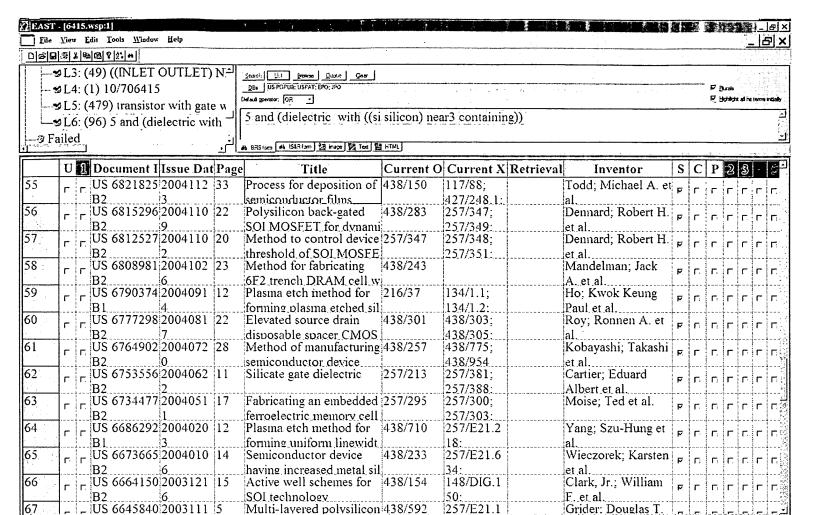
Ref #	Hits	Search Query	DBs	Default Operat or	Plural s	Time Stamp
L1	3564	((INLET OUTLET) NEAR3 PORTION) WITH (GAS LIQUID) WITH CHAMBER	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 14:58
L2	1831	((INLET OUTLET) NEAR3 PORTION) WITH (GAS LIQUID) WITH CHAMBER.CLM.	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 14:58
L3	49	((INLET OUTLET) NEAR3 PORTION) WITH (GAS LIQUID) WITH CHAMBER WITH CIRCULAR.CLM.	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 15:23
L4	1	10/706415	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 15:33
L5	479	transistor with gate with ((si silicon) near3 containing)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 15:38
L6	96	5 and (dielectric with ((si silicon) near3 containing))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/03/08 15:39

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L6: (96) 5 and (dielectric with	5 and (dielectric wit	h ((si silicon) near3 containing))		
U 1 Document I Issue Dat Pa	ge Title	Current O Current X Retrieval	Inventor	SCP23 E

50	8 L	2001005141 US 2001004025	2001111		Spot-implant method for MOS transistor application				Wasshuber,	_	_ i				-
4	PГ	US 2001004025	2001111			i			Christoph	1.	Г	Г	۲	ΓļΓ	r
	p r	2001004025		ì	SEMICONDUCTOR	257/314	257/E29.1		KOBAYASHI,	г	Г	Г.	r	rr	r
51		US	2001091			438/201	65: 257/E21.6		TAKASHI et al. KELLER, J.	г.	г.	г.	г	- r	-
		2001002154 US 6864125			ENHANCING DATA RE Process for growing a		82: 427/255.27		DENNIS et al.					 	
53		B2 US 6844234	8 2005011		dielectric laver on a silico Semiconductor device	438/287	: 438/591:	· ·	Singh et al. Eguchi; Kazuhiro et		أ			- - - -	
	! .	B2 US 6835983	8		and method for manufact Silicon-on-insulator		438/780: 257/348:		al. Ning; Tak H. et al.					{	
		B2 US 6821825		ì	(SOI) integrated circuit (I	} 	257/349:				,	1		1	Г.
		:B2	.3		Process for deposition of semiconductor films		117/88; 427/248.1:	1	Todd; Michael A. et al.		:			2	į
		US 6815296 B2	9	-	Polysilicon back-gated SOI MOSFET for dynami		257/347; 257/349:		Dennard; Robert H. et al.		. ?			1	
57	ĻГ	US 6812527 B2	2004110	20	Method to control device threshold of SOI MOSFE	257/347	257/348; 257/351:		Dennard; Robert H. et al.	Þ	г	г	г	r r	Ī-, -
58	гг	US 6808981 B2	2004102 6	23	Method for fabricating 6F2 trench DRAM cell w	438/243			Mandelman; Jack A. et al.	무	г	Г	г	r	r
59	гг	US 6790374 B1	2004091 4	12	Plasma etch method for forming plasma etched sil	216/37	134/1.1; 134/1.2:		Ho; Kwok Keung Paul et al.	F	г	r.	г	г	П
60	ГГ	US 6777298 B2	2004081	22		438/301	438/303; 438/305:		Roy; Ronnen A. et	F	г	Г	г	ר	r
61	حرا ہے	US 6764902	2004072	28	Method of manufacturing		438/775:		ar. Kobavashi: Takashi	. •	-	 ,	- - - -	15-
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68	г US 6620719 В1	6	1	Method of forming ohmic contacts using a self dopi		257/E21.4 13:	de la ma debate de constitue de	Andry; Paul Stephen et al.	ᄝ	г	пГ	- _	Г	<u></u>
69	г г US 6607946 В1	2003081 9	5		438/142	257/E21.1 93:		Sandhu; Gurtej Singh et al	Þ	г	n r	- [г	г.
70.	US 6596648	2003072	83	Material removal method	438/745	257/E21 0		Wu: Zhiqiang et al		_ 1	_	_ T		

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68	г	r US	6620719	2003091	14	Method of forming ohmic	438/597	257/E21.4	4	Andry; Paul	무	г	г	г	r r	Tr.
	[BL		6		contacts using a self dopi		13:		Stephen et al.				Ļ		
69	-	_ US	6607946	2003081	5	Process for growing a	438/142	257/E21.1		Sandhu; Gurtej	Þ	г.	п	_		· [r]
		B1		9		dielectric laver on a silico		93:		Singh et al.					.] .	
70.	_	_ US	6596648	2003072	83	Material removal method	438/745	257/E21.0		Wu; Zhiqiang et al.	_	Б	_	_	_ _	- r
	<u>.</u> [B2		2	L	for forming a structure		11:							<u>' </u>	
71.	<u></u>	_ US	6596585	2003072	28	Method of manufacturing	438/257	257/E29.1		Kobayashi; Takashi	5	_	Е	-	гг	
		B2		2		semiconductor device		65:		et al.	,				<u>' '</u>	
72	_ !	_ US	6566210	2003052	8	Method of improving gate		257/344;		Ajmera; Atul C. et		-	_	_	_	· [
3	1	B2		0	i	activation by employing a		257/E21.1		al.	"	'			<u>'</u>	
73	_	_ US	6548874	2003041	16	Higher voltage transistors	257/371	257/344;		Morton; Alec et al.	E	_	г	_	_ _	ГΕ
		BI		5		for sub micron CMOS pr		257/408:			Γ.	•			`	
74		- US	6521963	2003021	35	Semiconductor device	257/412	257/324;		Ota; Kazunobu et	-	_	_	_		· lnii
	!	BL		8		and method of manufactu		257/350:	i i	al.	'	1.		'		
75	_	_ US	6514843	2003020	8			257/E21.3		Dokumaci; Omer et	-	_	_	_		. _ []
	•	B2		4		oxidation of MOS transist		35:		al.		,		'		1.0
76		_ US	6489649	2002120	29	Semiconductor device	257/314	257/315;		Kobayashi; Takashi	_	_	_	_		· r
	1	B2		3		having nonvolatile memo		257/316:	,	et al.	<u>'</u>			'	<u>' </u>	
77		_ US	6469350	2002102	13	Active well schemes for	257/349	257/347;		Clark, Jr.; William	-	_	_	_		т.
		B1		2		SOI technology		257/354:		F, et al.	'	•	• :	•		
78		_ US	6462403	2002100	12	Semiconductor device	257/640	257/350;		Uochi; Hideki	_	_	_	_		· m
- v: 1		B1	;	8		comprising thin film trans		257/59:	-		'	•	• :	'	' ! '	
79		_ US	6458666	2002100	5	Spot-implant method for		438/525;		Wasshuber;	F	_	Γ.	_		r Š
100		B2		1		MOS transistor applicatio		438/531		Christoph	Ľ	'		'	' <u>i</u> '	
80		_ US	6444584	2002090		Plasma etch method for		438/710:		Hsiao: Yung-Kuan		,	. سر			<u>تر</u> ــال
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83	-	_	US 637957	5 2002043	16	Treatment of etching	216/67	134/1.1;		Yin; Gerald Zheyao	_			ĮΠ	ГГ	
 	լ՝		B1	0		chambers using activated		438/727: 4		et al.	i			<u>[</u>	<u> </u>	
84	P	Г	US 635290	0[2002030	5	Controlled oxide growth	438/305	257/E21.4		Mehrotra; Manoj et	г	r	Г	r	ר : ר	- Г
		ļ	BL	5		over polysilicon gates for		35:		al,	ļ	ļļ				-
85	무	г	US 625172	9 2001062	9	Method of manufacturing	438/257	257/204;		Montree; Andreas	г	Г	Г	г	r r	т.
		ļ 	B1	16		a nonvolatile memory	120/262	257/206:		H. et al.	ļ	ļļ				
86	Þ	г	US 619770	1 2001030	9	Lightly nitridation	438/763	257/E21.2		Shue; Shau-Lin et	г	г	r.	г	רר	Г.
87			US 617730	32001012	-	surface for preparing thin Method of manufacturing		68: 257/E21.4	}	aı. Schmitz; Jurriaan et		ļ <u>ļ</u>		-+		
67	P	Г	03 017730	:2	١	a semiconductor device w	1	35:		ol al	Г	Г	П	Г	רוְר	т.
88		!	US 613362	02000101	10			257/55;		Uochi; Hideki		l I		1::†	_ ; _	
	7	F	A	17		and process for fabricatin		257/57:			Г	「	Г	Г	רור	Γ
89	7	_	US 612463	8 2000092	47	Semiconductor device	257/751	257/384;		Iwasa; Shoichi	_		_		r r	
L			A	6	-	and a method of manufac		257/752:				[' '	
90	, p	-	US 589734	5 1999042	10	Semiconductor device	438/151	257/E21.2		Uochi; Hideki	r	٦	г	_	רוֹר	- г
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91	P	г	US 573123	8 1998032	8	Integrated circuit having a		257/E21.1		Cavins; Craig Allan	г	٢	г	г	ר וְר	- Г
II		ļ	A	4		liet vapor deposition silico		93:		et al.	ļ!					
92	P	Γ.	US 489469	3 1990011	12	Single-polysilicon dram	25 //511	257/384;		Tigelaar; Howard L.	٦	٦	г	Г	г	· r
93			A US 481107	61080030	20	device and process Integrated circuit device	257/311	257/915: 257/306;		et al.	ļ					
دوا	P	Г	3	7	20	and process with tin capa		257/300, 257/315:		Tigelaar; Howard L.	Г	r	Г	Г	רור	1 [5]
94			US 481107	6 1989030	111	Device and process with		257/311;		Tigelaar; Howard L.	†					
'	P	Γ.	A	7	1	doubled capacitors	23,,300	257/315:		et al	٦	ן ר	Г	Γ.	۲ ! ر	
95 1	7,	-	US 481067	3 1989030	9	Oxide deposition method	438/386	148/DIG.1		Freeman: Dean W.		_			جراب	لغرا
11.		- 1		3		The second second second			· · · · · · · · · · · · · · · · · · ·				, "	* -	-333	65 9 31